REMARKS

In the Final Office Action mailed May 3, 2006, claims 1, 5, 6 and 15-17 were rejected under 35 U.S.C. 102(e) as being anticipated by Datta (U.S. Patent No. 6,750,133); claims 2 and 3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Datta in view of Cheung (U.S. Patent No. 6,638,847); claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Datta in view of Darbha (U.S. Patent No. 5,904,555); and claims 14 and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Datta in view of Leibovitz (U.S. Patent No. 6,146,984). The foregoing rejections are respectfully traversed.

Claims 1 and 16 have been amended based upon the Examiner comments on page 6 of the Office Action.

Claims 1-6 and 14-18 are currently pending and under consideration. Reconsideration is respectfully requested. Claims 7-13 were withdrawn.

Claim 1 has been amended to recite "providing a wafer having a protective layer with an open electrode pad, the protective layer plating over the wafer excluding a portion of the wafer corresponding to the open electrode pad and the open electrode pad". Datta fails to discuss this feature.

Instead, Datta merely discusses a ball-limiting metallurgy stack for an electrical device that contains at least one copper layer disposed upon a titanium adhesion metal layer. The stack resists tin migration toward the upper metallization of the device (see Abstract). Datta further discusses an etch process flow which resists the re-deposition of the tin during etching of a copper layer. In FIG. 1, Datta illustrates a semiconductor structure including a substrate 12 and a metallization 14 such as a copper pad which makes connection to metal six (M6) or metal seven (M7), for example. The metallization 14 is coplanar with an upper surface 16 of the substrate. A nitride layer 18 is formed over the substrate 12 and the metallization 14. In addition, a passivation layer 20 is formed over the nitride layer 18 whereby the passivation layer 20 and the nitride layer 18 act to protect the substrate and to expose the metallization according to patterning (see column 2, lines 47-65, for example). Patterning is accomplished by use of a first mask to form a recess 22 during an etch process (see column 3, lines 4-9, for example).

Again, the present invention does not include a nitride layer 18 as in Datta. Nor does the present invention require an etching process in order to achieve a recess 22 as in Datta.

Instead, as mentioned above, the present invention discusses "the protective layer plating over the wafer excluding a portion of the wafer corresponding to the open electrode pad and the open electrode pad," as recited in amended claim 1, for example.

Independent claim 16 has been amended to recite features somewhat similar to those recited in amended claim 1, for example.

Claims 5, 6, 15 and 17 are dependent upon independent claims 1 and 16, respectively. Therefore, the comments mentioned above may be applied here also.

Regarding the 103(a) rejections:

Claims 2, 3, 4, 14 and 18 are dependent from claims 1 and 16, respectively. Therefore, the comments mentioned above regarding claims 1 and 16, may also be applied here.

In addition, Cheung, Darbha and Leibovitz each fail to make up for the deficiency of Datta mentioned above.

Instead, Cheung merely discusses a method of forming solder bumps on a chip whereby the solder bumps comprise pure tin or a tin alloy selected from tin-copper, tin silver, tin-bismuth or tin-silver-copper (see Abstract).

Further, although Darbha discusses a temperature and a time duration of a reflow process is determined in accordance with the type of device formed on a die 12, the composition of the solder bums, and the melting temperature of a glass sleeve, Darbha fails to make up for the deficiency of Datta as mentioned above.

Further, Leibovitz merely discusses uniform height solder bumps on a wafer created by exposing a dummy pattern of under bump metal for solder plating. The dummy pattern of exposed under bump metal follows the outer edge outline of a pattern of die that exists on the semiconductor wafer. The dummy pattern of under bump metal is exposed by removing a portion of a layer of photoresist that is deposited over the under bump metal (see Abstract).

Thus, the combination of Datta with any one of the above references fails to establish a prima facie case of obviousness over the present invention, as recited in amended claim 1, for example.

Therefore, claims 1-6 and 14-18 patentably distinguish over the cited references.

According, withdrawal of the foregoing rejections is respectfully requested.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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